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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,998	12/11/2003	Michael DeMar Taylor	DATUMTE.015A	8286

20995 7590 12/14/2005

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,998	TAYLOR ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are presented for examination.

2. The IDS filed on 12/11/2003 has been received and carefully considered.

Claim Objections

3. Claims 6 and 7 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. A microprocessor that is not currently operating according to the method of claim 1 (even though it is fully capable of doing so) would appear to infringe claim 6 and claim 7. Therefore, claims 6 and 7 are rejected under 112, 4th paragraph. See MPEP 608.01(n).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

4. Claims 6 and 7 are rejected under 112, 4th paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. A

microprocessor which is not currently operating according to the method of claim 1 (even though it is fully capable of doing so) would appear to infringe claim 6 and claim 7. Therefore, claims 6 and 7 are rejected under 112, 4th paragraph. See MPEP 608.01(n).

Drawings

5. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3-11 are rejected under 35 U.S.C. 102(e) as being anticipated by the 'Background of Invention' section of this application, hereinafter, BOI.

As per claim 1, BOI teaches a method of processing a memory read request from a central processing unit (CPU) of a microprocessor, the method comprising: retrieving a cache tag associated with the memory read request from a cache memory bank (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) that is external to the microprocessor, wherein the cache memory bank stores cache tags and cache data in separate memory locations; within the microprocessor, comparing the cache tag to a memory address associated with the memory read request to assess whether data requested by the CPU resides within the cache memory bank, and subsequent to retrieving the cache tag from the cache memory bank, accessing the cache memory bank to retrieve the cache data associated with the memory read request (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

As per claim 3, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the cache tag and the data are retrieved from the cache memory bank over a shared data/address bus that connects the microprocessor to the cache memory bank (e.g. see Fig. 4).

As per claim 4, BOI teaches the claimed invention as described above and furthermore, BOI teaches that comparing the cache tag to the memory address within a system controller device that interfaces the microprocessor to a main memory (e.g. see Fig. 4).

As per claim 5, BOI teaches the claimed invention as described above and furthermore, BOI teaches that the comparison circuitry identifies whether the memory address supplied by the microprocessor matches the data resident in the level 2 cache, which is similar to mapping the memory address, supplied by the microprocessor, into a cache tag address and a cache data address that are sequentially provided to the cache memory bank to retrieve the cache tag and the cache data therefrom (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

As per claim 6, BOI teaches a microprocessor (shown in Fig. 4) that operates according to the method of claim 1 (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

As per claim 7, BOI teaches the claimed invention as described above. The further limitation of, having an address transformation circuit that converts the memory address into cache memory addresses for reading the cache tag and cache data, in inherently embedded in the microprocessor taught by BOI. The Fig. 4 of BOI clearly shows that the microprocessor provides the cache index (i.e. the cache memory address) to the cache data and tag memories (e.g. see Fig. 4). Therefore, there has to be an address transformation circuit present in the microprocessor taught by BOI to convert the memory address into the cache index (i.e. the cache memory address) for reading the cache tag and cache data.

As per claim 8, BOI teaches a microprocessor system, comprising a bank (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) of general purpose random access memory that stores both cache tags and cache data in separate memory locations; and a microprocessor connected to the

bank of general purpose random access memory, and configured to use the bank of general purpose random access memory as an external cache memory; wherein the microprocessor is configured to retrieve a cache tag from the bank of general purpose random access memory before retrieving corresponding cache data from the bank of general purpose random access memory (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

As per claims 9-11, see arguments with respect to the rejection of claims 5, 3 and 4, respectively. Claims 9-11 are also rejected based on the rationale as the rejection of claims 5, 3 and 4, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Steely, Jr. et al. (USPN: 5,235,697) hereinafter, Steely.

As per claim 2, BOI teaches the claimed invention as described above. However, BOI does not teach that the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing the cache tag to the memory address. Steely, on the other hand, teaches that the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing

the cache tag to the memory address (e.g. see Col. 4, lines 12-20). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the feature taught by Steely in the method taught by BOI so by performing parallel operations, it permits the CPU to immediately use the data from the predicted data RAM, before completion of the tag comparison but subject to later receipt of a mis-predict signal indicative of an incorrect prediction by the set prediction RAM. In other words, in case if the cache tag does match with the memory address, i.e. cache hit, then the requested data is retrieved faster from the data RAM by performing the look-ahead step, i.e. starting the data retrieval step before finishing the tag compare step. In doing so, the data latency will be reduced and therefore, the overall performance of the microprocessor increases.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER